LOW VOLTAGE DIFFERENTIAL SIGNALING DRIVING APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a low voltage differential signaling (LVDS) driving apparatus, and more particularly, to a LVDS driving apparatus with low operation power.

2. Description of Related Art

FIG. 1 and 2 show a conventional configuration of an LVDS driving circuit. The conventional LVDS driving circuit sets in the receiving end 17 includes four transistors 10, 11, 12, 13, and two current sources 14, 15, as shown in FIG. 1 and 2. The ON/OFF status of the transistors 10 and 13 are controlled by the control signals S1, and that of the transistors 11 and 12 are controlled by the control signals S2. When the control signal S1 is LOW and S2 is HIGH, transistors 11 and 12 are ON and transistors 10 and 13 are OFF. Thus, a downward current is produced at the resistor 16 of the output-end 17 and an output logic "1" is produced based on the download current, as shown in FIG. 1. When the control signal S1 is HIGH and S2 is LOW, transistors 11 and 12 are OFF and transistors 10 and 13 are ON. Thus, a upward current is produced at the resistor 16 of the output-end17 and an output logic "0" is produced based on the upload current, as shown in FIG. 2.

However, the power source VDD of the conventional LVDS driving

circuit has to meet the limitation that VDD > $\Delta V_{14}+\Delta V_{15}+I_{ref}R_L+\Delta V_{11}+\Delta V_{12}$, wherein ΔV_{14} and ΔV_{15} are voltage drop of the current sources 14 and 15 respectively, and ΔV_{11} and ΔV_{12} are drain-to-source voltage drop of the transistors 11 (or 10) and 12 (or 13) respectively. That is, the minimum operational power VDD of the LVDS driving circuit must be no smaller than$\Delta V_{14}+\Delta V_{15}+I_{ref}R_L+\Delta V_{11}+\Delta V_{12}$, which is a relative large operational power requirement in a common integrated circuit. In addition, a complicated control circuit is needed to precisely control the current sources 14 and 15 such that the output current of the current sources 14 and 15 can be substantially the same.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a low voltage differential signaling (LVDS) driving apparatus which the magnitude of the operation power can be reduced and the control circuit of the LVDS driving apparatus can be simplified.

To achieve the object, a low voltage differential signaling (LVDS) driving apparatus is disclosed, which comprises an LVDS output circuit to output an LVDS differential signal; a switch circuit coupled to the LVDS output circuit to control the phase of the LVDS differential signal; and a reference current control circuit to provide a control voltage to the LVDS output circuit such that the magnitude of the LVDS differential signal is determined based on the control voltage.

Other objects, advantages, and novel features of the invention will

become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a conventional LVDS driving circuit, which an output logic "1" is produced at the output-end;

FIG. 2 shows a conventional LVDS driving circuit, which an output logic "0" is produced at the output-end;

FIGS. 3 is a block diagram of an LVDS driving circuit according to the embodiment of the present invention;

FIG. 4 is an example circuitry of an LVDS driving circuit of FIG. 3 according to the embodiment of the present invention;

FIG. 5 is an example circuitry of an LVDS driving circuit of FIG. 4, which an output logic "1" is produced at the output-end;

FIG. 6 is an example circuitry of an LVDS driving circuit of FIG. 4, which an output logic "0" is produced at the output-end; and

FIG. 7 is an example circuitry of the reference current control circuit according to the embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 3 is a block diagram of an LVDS driving apparatus according to the embodiment of the present invention. The LVDS driving circuit based on the embodiment of the present invention includes a differential signal output circuit 20, a switch circuit 30, a switch control circuit 40, and a reference current control circuit 50, as shown in FIG. 3. The differential signal output circuit 20 is for outputting an LVDS differential signal. The

switch circuit 30 coupled to the differential signal output circuit 20 is for controlling the differential signal output circuit 20 to output the desired LVDS differential signal. The switch control circuit 40 coupled to the switch circuit 30 is for controlling the operation of the switch circuit 30 through outputting a first control signal S1 and a second control signal S2. The reference current control circuit 50 coupled to the differential signal output circuit 20 and the switch circuit 30 for providing a first control voltage V1 and a second control voltage V2.

FIG. 4 is an example circuitry of an LVDS driving circuit of FIG. 3 according to the embodiment of the present invention. The differential signal output circuit 20 includes four transistors 21, 22, 23, and 24. The transistor 21 and 23 are PMOS transistors coupled to a operational voltage source VDD, and the transistor 22 and 24 are NMOS transistors coupled to the ground. The transistor 23 and 24 are coupled to the first output node and the transistor 21 and 22 are coupled to the second output node of the differential signal output circuit 20. The first and the second output node are for outputting an LVDS differential signal.

In this embodiment, the switch circuit 30 includes eight switches 31~38, as shown in FIG. 4. The switch 31 is coupled to the PMOS transistor 21 and the first output node of the reference current control circuit 50, the switch 33 is coupled to the NMOS transistor 22 and the second output node of the reference current control circuit 50, the switch 35 is coupled to the PMOS transistor 23 and the first output node of the reference current control circuit 50, and the switch 37 is coupled to the NMOS transistor 24

and the second output node of the reference current control circuit 50. In addition, the switch 32 is coupled to the operational voltage source VDD and the PMOS transistor 21, the switch 34 is coupled to the ground and the NMOS transistor 22, the switch 36 is coupled to the operational voltage source VDD and the PMOS transistor 23, and the switch 38 is coupled to the ground and the NMOS transistor 24. The switches 32, 33, 35, and 38 are controlled by the first control signal S1 and the switches 31, 34, 36, and 37 are controlled by the second control signal S2.

FIG. 5 is an example circuitry of an LVDS driving circuit of FIG. 4, which an output logic "1" is produced at the output-end. When the control signal S1 is HIGH and S2 is LOW, the switches 32, 33, 35, and 38 are ON and the switches 31, 34, 36, and 37 are OFF, as shown in FIG. 5. In this manner, the gate of the PMOS transistor 21 is coupled to the operational voltage source VDD and the gate of the NMOS transistor 24 is coupled to the ground, thus the PMOS transistor 21 and the NMOS transistor 24 are both OFF. Besides, the PMOS transistor 23 and the NMOS transistor 22 are ON through the controlling of the first control voltage V1 and the second control voltage V2 respectively. The LVDS differential signal in a positive phase is provided such that an output logic "1" is generated by the output-end based on the positive phase LVDS differential signal.

FIG. 6 is an example circuitry of an LVDS driving circuit of FIG. 4, which an output logic "0" is produced at the output-end. When the control signal S1 is LOW and S2 is HIGH, the switches 32, 33, 35, and 38 are OFF and the switches 31, 34, 36, and 37 are ON, as shown in FIG. 6. In this

manner, the gate of the PMOS transistor 23 is coupled to the operational voltage source VDD and the gate of the NMOS transistor 22 is coupled to the ground, thus the PMOS transistor 23 and the NMOS transistor 22 are both OFF. Besides, the PMOS transistor 21 and the NMOS transistor 24 are ON through the controlling of the first control voltage V1 and the second control voltage V2 respectively. The LVDS differential signal in a negative phase is provided such that an output logic "0" is generated by the output-end based on the negative phase of the LVDS differential signal.

The operational voltage source VDD of the LVDS driving circuit shown in FIG. 4 has to meet the limitation that $VDD > I_{ref}R_L+\Delta V_{23}+\Delta V_{22}$, wherein ΔV_{23} and ΔV_{22} are the drain-to-source voltage drops of the transistors 23 (or 21) and 22 (or 24) respectively. That is, the minimum operational power VDD of the LVDS driving circuit must be no smaller than $I_{ref}R_L+\Delta V_{23}+\Delta V_{22}$, which is much smaller compared to that of the conventional LVDS driving circuit shown in FIG. 1. In addition, since there are no current sources in the LVDS driving circuit shown in FIG. 4, a complicated control circuit is not needed to precisely control the output current of the current sources.

FIG. 7 is an example circuitry of the reference current control circuit according to the embodiment of the present invention. The reference current control circuit 50 is for providing the first control voltage V1 and the second control voltage V2 to the transistors 21~24 of the differential signal output circuit 20 to control either the PMOS transistor 21 and the NOS transistor 24 or the PMOS transistor 22 and the NOS transistor 23 to

operate in the triode region. In this manner, the magnitude of the LVDS differential signal outputted from the differential signal output circuit 20 can be controlled through controlling the magnitude of the first control voltage V1 and the second control voltage V2 provided by the reference current control circuit 50. In FIG. 7, the reference current control circuit 50 includes an operational amplifier 51, a current source 52, a first resistor 53, a second resistor 54, the PMOS transistors 56 and 57, and a NMOS transistor 55. Since the transistors 55, 56, and 57 are manufactured through the same manufacturing process, the $\mu_n C_{ox}$ value of the transistors 55, 56, and 57 are substantially the same. Thus, through controlling the W/L ratio of the transistors 55, 56, and 57 (i.e., $\frac{W_{56}}{L_{56}} : \frac{W_{57}}{L_{57}} : \frac{W_{55}}{L_{55}} = 1 : n : m$), the currents across the transistors 55 and 56 can be controlled as I_{ref}/n. Accordingly, the first control voltage V1 and the second control voltage V2 can be determined.

Although the present invention has been explained in relation to its preferred embodiment, it is to be understood that many other possible modifications and variations can be made without departing from the spirit and scope of the invention as hereinafter claimed.